IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ziedman, Robert M.
Title:	System And Method for Connecting A Logic Circuit Simulation To A Network

Serial No.:	10/044,217	Filing Date:	November 19, 2001

Confirmation No.: 9153

Examiner:	Unassigned	Group Art Unit:	Unassigned

Docket No.:   M-8637-1P US

San Jose, California
April 8, 2002

Box Missing Parts
Attn: Official Draftsperson
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicant submits eight (8) sheets of formal drawings, consisting of Figures 1, 2, 3, 4, 5, 6, 7, 8 and 9, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (408) 453-9200.

EXPRESS MAIL LABEL NO:
EL 937084330 US

Respectfully submitted,

Norman R. Klivans
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